WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a substrate;

an insulating layer formed on the substrate;

a fin formed on the insulating layer;

a source region formed on the insulating layer adjacent a first side of the fin; and

a drain region formed on the insulating layer adjacent a second side of the fin opposite the first side, wherein the source and drain regions have a greater thickness than the fin.

2. The semiconductor device of claim 1, wherein the fin has a thickness ranging from about 500 Å to about 800 Å in a channel region of the semiconductor device.

3. The semiconductor device of claim 2, wherein the source region and drain region each has a thickness ranging from about 700 Å to about 1000 Å.

4. The semiconductor device of claim 1, wherein the fin has a width ranging from about 50 Å to about 200 Å in a channel region of the semiconductor device.

5. The semiconductor device 1, further comprising:

a gate formed over a top surface of the fin in a channel region of the semiconductor device.

6. The semiconductor device of claim 5, wherein the gate comprises a first gate disposed on a third side of the fin and a second gate disposed on a fourth side of the fin opposite the third side.

7. The semiconductor device of claim 1, further comprising:

at least one dielectric layer formed over a top surface of the fin.

8. The semiconductor device of claim 7, further comprising:

a gate formed over the at least one dielectric layer and being disposed on a third and fourth side of the fin.

9. The semiconductor device of claim 1, wherein the insulating later comprises a buried oxide layer and the fin comprises at least one of silicon and germanium.

10. A method of manufacturing a semiconductor device including, comprising:

forming a first mask over a silicon on insulator (SOI) wafer, the SOI wafer comprising a conductive layer on an insulating layer that is formed on a substrate;

etching a portion of the conductive layer to form a fin structure;

forming a source region and drain region adjacent respective ends of the fin structure;

forming a second mask over the source region and drain region;

etching the fin structure to reduce the width and thickness of the fin structure;

depositing a gate material over the fin structure; and

patterning and etching the gate material to form a gate electrode.

11. The method of claim 10, wherein the etching the fin structure comprises:

isotropically etching the fin structure in a channel region of the semiconductor device.

12. The method of claim 11, wherein the etching the fin structure comprises:

using a wet etch chemistry to reduce the width and thickness of the fin structure such that the fin has a smaller thickness than the source and drain regions.

13. The method of claim 10, further comprising:

implanting impurities in the source and drain regions; and

annealing the semiconductor device to activate the source and drain regions.

14. The method of claim 10, further comprising:

forming a dielectric layer over the fin structure prior to depositing the gate material, the dielectric layer having a thickness ranging from about 10 Å to about 20 Å.

15. A semiconductor device, comprising:

a substrate;

an insulating layer disposed on the substrate;

a conductive fin formed on the insulating layer, the conductive fin having a first end and a second end;

a source region formed adjacent the first end of the conductive fin; and

a drain region formed adjacent the second end of the conductive fin, wherein the source and drain regions have a greater thickness than the conductive fin in a channel region of the semiconductor device.

16. The semiconductor device of claim 15, further comprising:

a gate dielectric layer formed on the conductive fin in the channel region of the semiconductor device; and

a gate formed over the gate dielectric layer.

17. The semiconductor device of claim 16, wherein the gate comprises a first gate electrode disposed on a first side of the conductive fin and a second gate electrode disposed on a second side of the conductive fin opposite the first side.

18. The semiconductor device of claim 15, wherein the conductive fin has a thickness ranging from about 500 Å to about 800 Å and a width ranging from about 50 Å to about 200 Å in the channel region of the semiconductor device.

19. The semiconductor device of claim 18, wherein the source region and drain region each have a thickness ranging from about 700 Å to about 1000 Å.

20. The semiconductor device of claim 15, wherein the source and drain regions are each at least about 200 Å thicker than the conductive fin in the channel region of the semiconductor device.